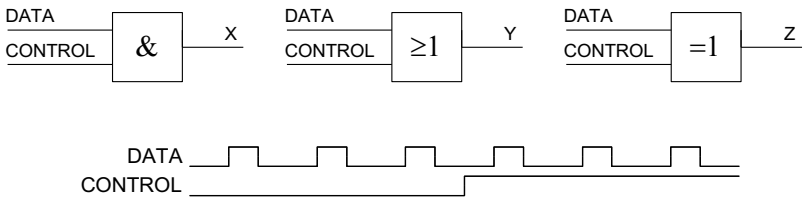
ELEC50001 EE2 Circuits and Systems

Problem Sheet 3

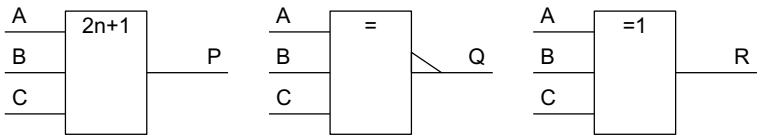
(FPGA basics and SystemVerilog – Lectures 7 & 8)

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

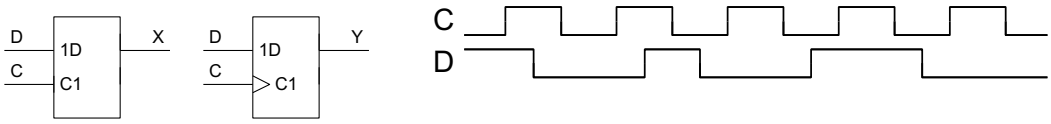
1A. The diagram shows three gates in which one input (CONTROL) is being used to modify a signal at the other input (DATA). Complete the timing diagram by drawing the waveforms of X, Y and Z. Describe in words the effect each of the gates has on DATA when CONTROL is low and when it is high.



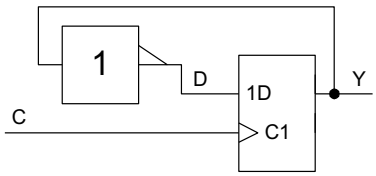
1B. The symbol in a gate generally indicates how many of the inputs need to be high to make the output high. Guess the truth tables of the following gates from their symbols. Explain why any one of them could be considered as a 3-input XOR gate.



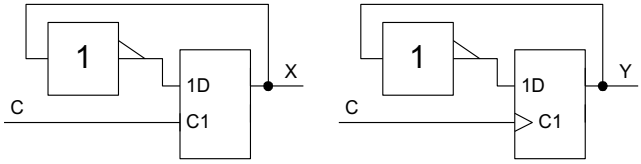
2A. The circuits below are a D-latch and a D-flipflop. Complete the timing diagram by drawing the waveforms of X and Y assuming that they are both low initially.



3B. The circuit below forms a ÷2 counter. If the inverter has a propagation delay of 5 ns and the propagation delay, setup time and hold time of the flipflop are 8 ns, 4 ns and 2 ns respectively, calculate the highest clock frequency for reliable operation.

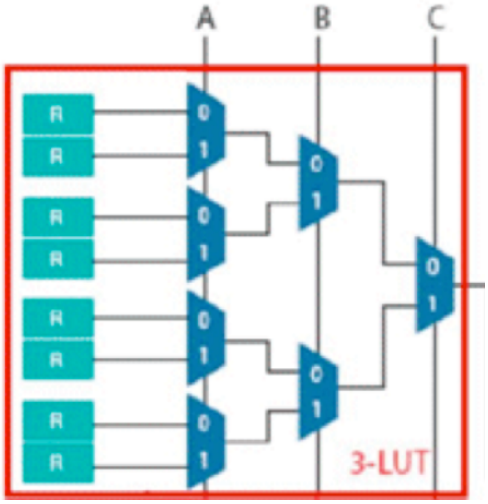


4B. The circuits below are a D-latch and a D-flipflop with their outputs connected to their inputs via an inverter. Draw the waveforms of X and Y assuming that they are both low initially and that C is a uniform square wave. (One of these circuits is a disaster and should never be used.)



5A. The 3-input Look-up Table (LUT) circuit could be made up from seven 2-to-1 multiplexers as shown here. Determine the configuration bits that must be stored in the eight registers driving this 3-LUT in order to implement the Boolean function:

$$Y = A*\sim C + \sim B*C + \sim A*B$$



6B. Design in SystemVerilog HDL the hardware module LE_3LUT that implements the 3-LUT circuit shown above.

7B. This is the 4-LUT circuit similar to that found in the Logic Element of an MAX10 FPGA. What is the bits that are stored in the registers during configuration in order to implement the following Boolean equation? You can assume that {D,C,B,A} = in[3:0] and Y = out[6]. (note: to simplify writing equations, I sometimes drop the brackets: out[6] becomes out6.)

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out6 = ~in3*~in2*~in1 + in3*in2*~in1*~in0 + ~in3*in2*in1*in0
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